REMARKS

Claims 1-8 stand examined and are rejected on various grounds, which are each addressed below. By virtue of this response, no claims are amended, no claims are added, and no claims are cancelled. Therefore, claims 1-8 are presently under consideration.

In view of the preceding amendments and the remarks made herein, the present application is believed to be in condition for allowance.

35 U.S.C.§ 103(a)

Claims 1 and 5 stand rejected under 35 U.S.C. § 103 as being allegedly obvious over the AAPA (Applicant Admitted Prior Art), in view of U.S. Patent No. 5,381,369 to Kikuchi et al. (Kikuchi).

A portion of claim 1 is paraphrased for context in responding to the rejection. Claim 1 is to an "erroneous operation preventing circuit" for use in non-volatile memory devices for setting one or more operational modes. The modes include a first reading mode for reading data out from a memory array, a programming mode of writing data to the memory array, an erasing mode of erasing data from the memory array, and a second reading mode of reading out data not stored in the memory array. The modes are set in accordance with an input control command.

The Examiner cited Kikuchi, Col. 4, line 67 through Col. 5, line 2 and Col. 5, lines 26-27 and 37-41 for combining with the AAPA. Col. 4, lines 67 – Col. 5, line 2 provides that an object in Kikuchi is "a semiconductor memory device which has the protect function of inhibiting the device from writing and erasing data so that even if an erroneous command is taken in due to power noise or command noise, the command may not stand valid, and which thereby improves the operating margin."

Kikuchi Col. 5, lines 26-27 and 37-41 teaches "[a]ccording to the configuration of this invention, a protect memory cell is provided in a semiconductor chip using a command control

system. By reading the data from the protect memory cell whenever a command is executed, the device is inhibited from being written into or erased from if an erroneous command is taken in."

Kikuchi thus teaches a "protect memory cell" for inhibiting writing or erasing of cells due to erroneous commands "taken in." However, the Examiner further construed the above section as teaching "an operational mode enforcing circuit for setting the first reading mode regardless of the input control command, in a data protection status where the programming mode and the erasing mode are inhibited from being set in accordance with a control signal for protecting predetermined data" as recited in claim 1.

Kukuchi may suggest reading from a "protect memory cell" for inhibiting programming and erasure, even if a write or erase command is "taken in." However, the Applicants respectfully submit that Kikuchi does not teach or suggest setting the first reading mode, which is a mode of reading from the memory array where information such as programs and data are stored, regardless of the input control command, in a data protection status where the programming mode and the erase mode are inhibited.

Because the proposed combination of references do not teach or suggest all the limitations of claim 1, the Applicants respectfully request withdrawal of the rejection of claim 1.

Claim 5:

The Examiner cited FIG. 10 of Kikuchi. Applicants submit that Kikuchi does not teach or suggest, "setting an inner level of a control command input circuit to an inner level corresponding to the first reading mode regardless of an input level of the control command, in a data protection status where the programming mode and the erase mode are inhibited" as recited in claim 5. Claim 5, like claim 1, recites that the first reading mode is "of reading out data from a memory array." Because the proposed combination of references do not teach or suggest all the limitations of claim 5, the Applicants respectfully request withdrawal of the rejection of claim 5.

Claims 2-4, 6-8 stand rejected under 35 U.S.C. § 103 as being allegedly obvious over the AAPA (Applicant Admitted Prior Art), in view of U.S. Patent No. 5,381,369 to Kikuchi et al. in view of Japanese Patent Application 09-69066.

Claims 2-4 and 6-8 respectively depend from independent claims 1 and 5. Applicants submit that claims 1 and 5 are allowable over the proposed combinations of references at least because of the reasons described above. Applicants further submit that claims 2-4 and 6-8 are therefore allowable at least by virtue of dependency from those allowable claims, and request withdrawal of the rejections against each claim.

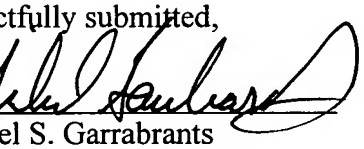
CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 577642000100. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: February 8, 2006

Respectfully submitted,

By 

Michael S. Garrabrants
Registration No.:51,230
MORRISON & FOERSTER LLP
755 Page Mill Road
Palo Alto, California 94304-1018
(650)813-4227

AMENDMENTS TO THE DRAWINGS

Replacement sheets effecting the following changes are included in this response.

In FIGS. 2, 5, 6, and 8 what was called the "WE# terminal" has been renamed the "WE# input terminal" for consistency with FIG. 4.

FIGS. 10a, 10b, and 11 have each been labeled "prior art."